BAJOPMAS JOURNAL 16(1):125 – 133
Printed in Bayero University, Kano - Nigeria.

COMPARATIVE THERMAL ANALYSIS Of Si-FinFET AND Si-NANOWIRE FET AT SUB-20NM NODE

[1*]Shehu, N. M.; [1]Galadima, B. Y. and [2]Ibrahim, M.
[1]Department of Physics, Bayero University, Kano, Nigeria
[2]Department of Physics, Northwest University, Kano, Nigeria
[*]Corresponding Author Email: nmshehu.phy@buk.edu.ng

ABSTRACT
Continuous downscaling of Complementary Metal Oxide Semiconductor (CMOS) technology has driven the development of advanced transistor architectures such as Fin Field-Effect Transistor (FinFET) and Nanowire Field-Effect Transistor (NWFET), designed to suppress short-channel effects (SCEs) and enhance current drive. However, at sub-20 nm technology nodes, temperature-induced performance degradation becomes increasingly critical. This paper presents a comparative evaluation of temperature effects on the electrical characteristics of Si-FinFET and Si-NWFET devices using the PADRE simulator. The parameters studied include Drain-Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Threshold Voltage (Vth), Transconductance (Gm), and On/Off current ratio (Ion/Ioff), analyzed for a temperature range of 250–500 K under identical structural and biasing conditions. Results show that Si-NWFET exhibits significantly improved electrostatic control, achieving 93.7% lower DIBL and 56.5% lower SS compared to Si-FinFET. Si-NWFET also demonstrates 300.7% higher Ion/Ioff, confirming superior switching and leakage performance. Conversely, Si-FinFET achieves ~94% higher transconductance and 79.17% lower Vth, indicating a much stronger current-driving capability and lower power consumption. These results highlight the performance trade-offs between both architectures and provide useful insight for optimizing device design in future nanoscale CMOS technologies.

Keywords: CMOS Technology, FinFET, Nanowire Field-Effect Transistor (NWFET), Short-Channel Effects (SCEs), Temperature Effects, Transconductance

1.0 INTRODUCTION
Continuous scaling of Complementary Metal Oxide Semiconductor (CMOS) has led to the development of advanced transistor structures such as Fin Field Effect Transistor (FinFET) and Nanowire Field Effect Transistor (NWFET) to address short channel effects (SCEs) [1], [2], [3], [4], [5], [6], [7] and improve current drive capability. Their superior electrostatic control and scalability have made them promising candidates for extending Moore's Law beyond CMOS technology. However, as the channel length is reduced below 20nm, confined geometries (FinFETs and nanowire FETs) exhibit pronounced self-heating and thermal degradation that materially affect device performance and reliability [8], [9],[10]; therefore, thermal/temperature studies are essential to evaluate transistor operation in practical, densely packed circuits.

Recent studies have examined temperature dependence in FinFET [11],[12],[13],[14] and SNWFET [1], [15], focusing on individual architectures. However, these investigations often differ in device geometry, material composition, or biasing conditions, making it difficult to directly compare thermal behavior across structures. Furthermore, systematic comparative studies of Si-FinFET and Si-NWFET devices under identical structures and bias condition remain limited in the current literature.

Unlike prior studies that examined each device independently, this work performed a direct comparative thermal analysis of Si-FinFET and Si-NWFET structures under identical structural and bias conditions. The study investigated the influence of temperature on their electrical characteristics and performance at sub-20 nm technology nodes, where thermal effects become increasingly dominant due to reduced channel dimensions. By employing device level simulations, critical temperature-dependent parameters such as DIBL, SS, Vth roll-off, Ion/Ioff and Gm were analyzed under varying temperature conditions. The result of the study provides valuable insight into the thermal stability and performance trade-offs between FinFET and NWFET devices, thereby contributing to the optimization of future nanoscale device designs for reliable and energy-efficient operation.

1.1 Theoretical Background

To provide a clearer understanding of the temperature-dependent behavior of the Si-FinFET and Si-NWFET devices, it is essential to establish the theoretical foundation underlying the key electrical parameters analyzed in this study. These parameters i.e. Drain-Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Threshold Voltage (Vth), Transconductance (Gm), and On/Off current ratio (Ion/Ioff) serve as critical indicators of short-channel effects, switching performance, and overall device efficiency in nanoscale transistors. The following subsections briefly present the governing equations and physical significance of each parameter as they relate to the thermal and electrostatic characteristics of the simulated deices.

(i) Drain-Induced Barrier Lowering (DIBL): This is one of the most critical short channel effect. The increase in drain voltage from 0.01 V to 0.05 V causes a variation in threshold voltage. This is referred to as drain induced barrier lowering. Drain-Induced barrier lowering is given by [16]:

$$DIBL\ (\frac{mV}{V}) = \frac{\Delta\, V_{TH}}{\Delta\, V_{DS}} \tag{1}$$

where V_{TH} denotes the threshold voltage and V_{DS} denotes the drain-source voltage. A lower DIBL value indicates stronger gate control and reduced short-channel effects.

(ii) Subthreshold Swing: The subthreshold swing parameter, one of the SCEs, for a Multigate Field Effect Transistor is usually 60 mV/dec. The SS can be calculated by [17]:

$$SS\ (mV/\,dec) = \frac{d\, V_{GS}}{d\ (log_{10}\ I_{DS}\ )} \tag{2}$$

where V_{Gs} denotes gate-source voltage and I_{DS} denotes drain-source current.

Lower subthreshold swing values are preferred in transistor design because they indicate improved switching efficiency, reduced power consumption, and enhanced overall device performance.

(iii) Threshold Voltage: The lowest gate voltage required to provide a conduction path between the source and the drain is known as the threshold voltage. Threshold voltage can be determined using [18]:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \tag{3}$$

where Q_{SS} denotes gate dielectric charge, C_{ox} is the capacitance in the gate, Q_D is the depletion charge in the channel, f_{ms} denotes metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential, and V_{in} is the additional surface potential to $2f_f$ that is required for ultrathin body devices to cause enough inversion charges in to the channel region of the transistor to reach threshold point [19].
Lower threshold voltage in nanoscale device operation is essential for reducing power consumption, improving performance, enabling further scaling, facilitating operation at lower voltages, and ensuring compatibility with modern low-voltage systems.

iv.Transconductance: The transconductance represents the rate of change of drain current with respect to variations in the gate–source voltage. As the donor ion concentration in the source and drain regions increases, the drain current I_D also rises gradually. This behavior can be attributed to the reduction in the device's effective channel length, caused by lateral diffusion from the source and drain regions [18]. Transconductance can be calculated by [20]:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{4}$$

where V_{GS} is the gate-source voltage and I_D is the drain current. A higher gm implies stronger current-driving capability and better channel conductivity.

2.0 METHODOLOGY

The simulations of FinFET and NWFET were performed using the PADRE simulator, an important simulator from a MUGFET tool developed by Purdue University readily available on nanoHUB. Researchers use this simulator to generate crucial curves that explain the basics of FETs. The simulator provides consistent solutions to the Poisson and drift-diffusion equations. The MuGFET simulator employs drift–diffusion modeling techniques to analyze nanoscale multi-gate FET architectures, such as Nanowire FETs and FinFETs. This approach is widely adopted by researchers to minimize performance losses in nanodevices, given the high fabrication cost of such devices and the extensive reliance on MuGFET-based simulations within nanoscale transistor research [12]. In the simulation of both devices; FinFET and NWFET (Figures 1 and 2), key structural parameters were maintained constant. The gate length was set to 10 nm, the gate oxide thickness to 1.5 nm, the gate/channel length to 10 nm, the channel width to 10 nm, the channel doping concentration to 1×10^{-16} cm^{-3}, and the source/drain doping concentration to 1×10^{-19} cm^{-3}. The drain bias was varied between 0.05 V and 1 V, while the gate bias was swept from 0 V to 1 V. The operating temperature was varied from 250 K to 500 K for both devices. Silicon (Si) was employed as the channel material, and silicon dioxide (SiO_2) served as the gate dielectric for both FinFET and NWFET structures.

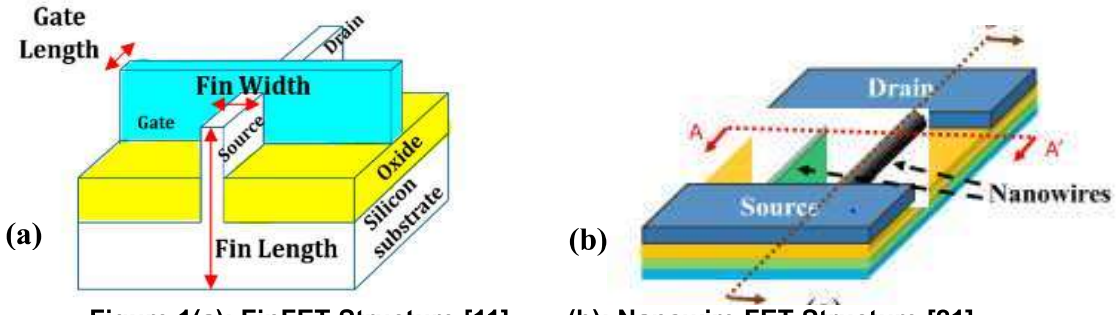

Figure 1(a): FinFET Structure [11], (b): Nanowire FET Structure [21].

3.0 RESULTS AND DISCUSSION

This section presents and discusses the simulated results of key device performance parameters, including Drain-Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Threshold Voltage Roll-off (Vth roll-off), On/Off Current Ratio (I_{on}/I_{off}), and Transconductance (Gm). These parameters are crucial indicators of the short-channel effects, switching efficiency, and overall electrical behavior of nanoscale transistors. The analysis of these parameters provides comprehensive insight into the electrostatic control, thermal stability, and overall performance of the studied devices under varying operating conditions.

3.1 Temperature Effect on Drain-Induced Barrier Lowering

Figure 2 illustrates the variation of Drain-Induced Barrier Lowering (DIBL) with temperature for both Si-FinFET and Si-NWFET devices. It is observed that the DIBL behavior exhibits distinct trends for the two device architectures across the temperature range of 250 K to 500 K. For the Si-FinFET, DIBL initially increases with temperature, reaching a peak at 450 K, and subsequently decreases beyond this point. In contrast, the Si-NWFET shows an increase in DIBL from 250 K to 400 K, followed by a decline as the temperature further rises to 500 K. Quantitatively, the Si-FinFET recorded the highest and lowest DIBL values of 382.78 mV/V and 349.88 mV/V at 450 K and 350 K, respectively. Meanwhile, the Si-NWFET exhibited a minimum DIBL of 21.94 mV/V at 250 K and a maximum of 81.38 mV/V at 450 K. The relatively low DIBL values obtained for Si-NWFET across the studied temperature range indicate its superior immunity to short-channel effects compared to the Si-FinFET. Notably, at 250 K, the Si-NWFET exhibited the least DIBL value of 21.94 mV/V, achieving 93.7% lower DIBL, confirming its enhanced electrostatic control and thermal stability under low-temperature operation. The result implies that Si-NWFETs exhibit superior thermal stability and stronger gate control compared to Si-FinFETs, as evidenced by their lower DIBL values across temperatures. This makes Si-NWFETs more suitable for low-power and high-performance applications where short-channel effects and temperature sensitivity are critical.

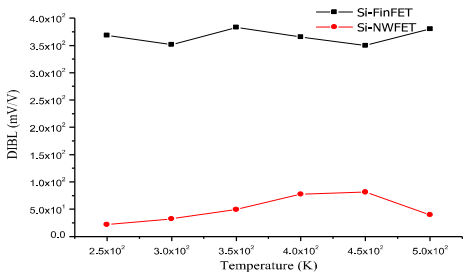

Figure 2: Drain Induced Barrier Lowering Vs Temperature

3.2 Temperature Effect on Subthreshold Swing

Figure 3 illustrates the variation of Subthreshold Swing (SS) with temperature for both Si-FinFET and Si-NWFET devices over the range of 250 K to 500 K. A general increase in SS with temperature is observed for both device architectures, indicating a degradation in subthreshold behavior as thermal energy rises. This trend reflects the increased carrier generation and reduced gate control at elevated temperatures. For the Si-FinFET, SS values range from a minimum of 153.79 mV/dec at 250 K to a maximum of 197.33 mV/dec at 300 K, with an almost constant value of 0 mV/dec recorded between 300 K and 500 K, as shown

in the figure. In contrast, the Si-NWFET demonstrates a minimum SS of 66.93 mV/dec, achieving a 56.5% lower SS at 250 K and a maximum of 160.39 mV/dec at 500 K. Comparatively, the Si-NWFET consistently exhibits lower SS values across the studied temperature range, signifying better subthreshold characteristics and enhanced switching efficiency. The lowest SS value of 66.93 mV/dec recorded at 250 K confirms the superior electrostatic integrity of Si-NWFET, implying faster switching and lower power dissipation than the Si-FinFET under similar thermal conditions.

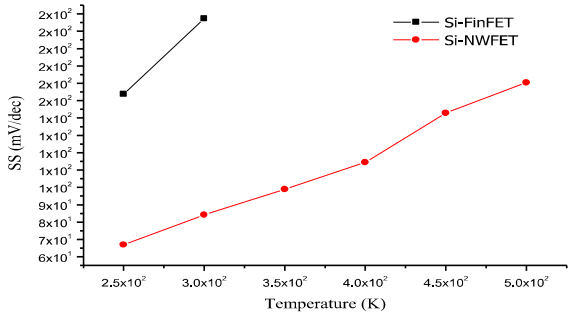

Figure 2: Subthreshold Swing Vs Temperature

3.3 Temperature Effect on Threshold Voltage Roll-off

Figure 4 illustrates the variation of threshold voltage (Vth) with temperature for both Si-FinFET and Si-NWFET devices. As observed, Vth decreases progressively with increasing temperature from 250 K to 500 K in both device types. This inverse relationship is attributed to enhanced carrier mobility and increased intrinsic carrier concentration at elevated temperatures, which collectively weaken the gate's control over the channel potential. Quantitatively, the Si-FinFET exhibits a maximum Vth of 0.27 V at 250 K and a minimum of 0.10 V, achieving a79.17% lower threshold voltage at 500 K than Si-NWFET. Similarly, the Si-NWFET demonstrates a maximum Vth of 0.57 V at 250 K and a minimum of 0.48 V at 500 K. However, the lower Vth value of 0.10 V recorded for the Si-FinFET at 500 K implies reduced power consumption, as devices with smaller threshold voltages require lower gate voltages to switch on. This characteristic makes the Si-FinFET more suitable for low-power applications, whereas the relatively higher Vth of Si-NWFET indicates stronger electrostatic control and enhanced stability against thermal variations.

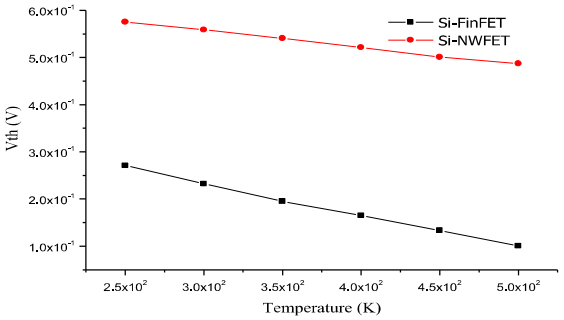

Figure 3: Threshold Voltage Vs Temperature

3.4 Temperature Effect on Transconductance

Figure 5 illustrates the variation of transconductance with temperature for both Si-FinFET and Si-NWFET devices. As shown in the figure, the transconductance of the Si-FinFET increases with rising temperature, indicating enhanced carrier mobility and improved channel conductivity at elevated thermal conditions. Specifically, the Si-FinFET demonstrated a minimum transconductance of 1.7×10^{-5} S/μm at 250 K and a maximum of 1.7×10^{-4} S/μm at 500 K. Conversely, the Si-NWFET exhibited a much lower transconductance response, with a minimum of 1.12×10^{-10} S/μm at 250 K and a maximum of 1.7×10^{-6} S/μm at 500 K.

The notable increase in transconductance with temperature for both devices suggests that thermal excitation enhances charge carrier activity; however, the Si-FinFET showed a significantly stronger dependence on temperature compared to the Si-NWFET. This can be attributed to its superior electrostatic control and higher effective channel mobility. Overall, the Si-FinFET exhibited the highest transconductance value of 1.7×10^{-4} S/μm achieving a 94% higher transconductance, at 500 K, confirming its better current-driving capability under high-temperature operation.

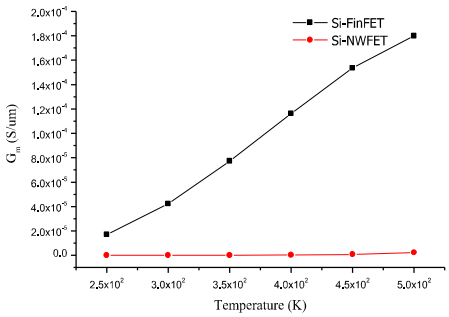

Figure 4: Transconductance Vs Temperature

3.5 Temperature Effect on I_{on}/I_{off} Current Ratio

Figure 6 presents the variation of the I_{on}/I_{off} current ratio with temperature for the simulated Si-FinFET and Si-NWFET devices within the temperature range of 250 K to 500 K. It can be observed that in the Si-FinFET, the I_{on}/I_{off} current ratio increases gradually from approximately 6.58 to 248.72 as temperature rises. The relatively small variation across the studied temperature range results in a nearly flat trend, indicating that the Si-FinFET maintains excellent thermal stability. This behavior suggests minimal sensitivity of the device's switching performance to temperature fluctuations, implying that strong electrostatic gate control effectively suppresses thermally induced current leakage.

In contrast, the Si-NWFET exhibits an inverse trend, where the I_{on}/I_{off} current ratio decreases with increasing temperature. At 250 K, the device demonstrated a maximum I_{on}/I_{off} of 2.8×10^{8}, which reduces to approximately 997 at 500 K. This pronounced decline indicates a higher susceptibility of the Si-NWFET to thermal effects, possibly due to enhanced carrier scattering and increased subthreshold leakage at elevated temperatures. A comparative assessment reveals that although the Si-FinFET exhibits better thermal stability, the Si-NWFET demonstrates a significantly higher I_{on}/I_{off} current ratio overall, reaching up to 2.8×10^{8}, achieving a 300.7% higher On/Off current ratio than Si-FinFET at low temperatures. This superior switching ratio highlights the enhanced current modulation

capability of the nanowire structure, making it more suitable for high-performance and low-power applications, albeit with slightly reduced thermal robustness compared to the FinFET.

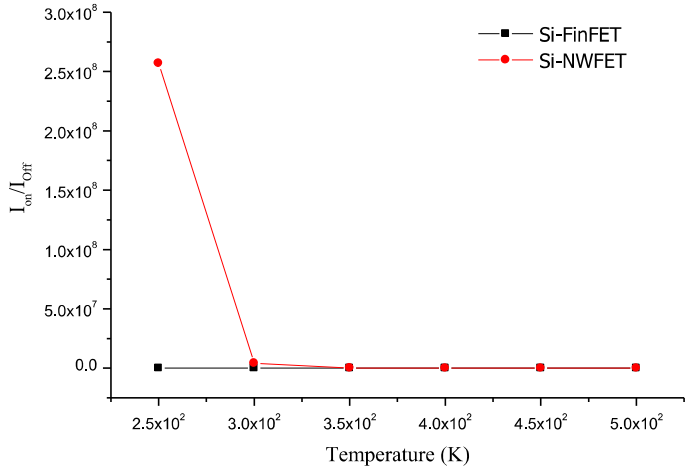

Figure 5: On/Off Current Ratio Vs Temperature

The overall performance comparison of Si-FinFET and Si-NWFET is summarized in Table 1, showing that Si-NWFET offers superior electrostatic control with 93.7% lower DIBL, 56.5% lower SS, and 300.7% higher Ion/Ioff ratio, indicating better switching and energy efficiency. Conversely, Si-FinFET exhibits 9894% higher transconductance and 79.17% lower threshold voltage, highlighting its stronger current drive, improved thermal stability, and reduced power consumption at high temperatures.

Table 1: Comparison of Si-FinFET and Si-NWFET Performance Parameter Si-FinFET Si-NWFET % Improvement (Better device) Observation

DIBL (mV/V)	349.88	21.94	97.3% (Si-NWFET)	Lower power cons.
SS (mV/dec)	153.79	66.93	56.5% (Si-NWFET)	Faster switching
Vth (V)	0.1	0.48	79.17% (Si-FinFET)	Lower power cons.
Gm (S/μm)	1.7×10^{-4}	1.7×10^{-6}	94% (Si-FinFET)	Superior drive cap.
I_{on}/I_{off}	248.72	997	300.7% (Si-NWFET)	Higher switching ratio

4. CONCLUSION

The comparative analysis of Si-FinFET and Si-NWFET under identical structural and biasing conditions revealed that each device exhibited distinct strengths depending on the intended application. The Si-NWFET demonstrated superior electrostatic control and switching behavior, achieving 93.7% lower Drain-Induced Barrier Lowering (DIBL) and 56.5% lower Subthreshold Swing (SS) than the Si-FinFET. It also maintained a 300.7% higher On/Off current ratio (Ion/Ioff), indicating enhanced resistance to short-channel effects, reduced leakage, and improved switching efficiency at lower operating temperatures. On the other hand, the Si-FinFET exhibited a remarkable 9894% higher transconductance, and 79.17% lower threshold voltage highlighting its stronger current-driving capability and higher speed and thermal stability under high temperatures. Overall, the findings establish that Si-NWFET is more suitable for low-power and energy-efficient applications, where minimal leakage and superior electrostatic control are prioritized, while Si-FinFET is better optimized for high-

speed and thermally demanding operations. This comparative study provides essential insights into the temperature-dependent behavior of nanoscale transistor architectures and serves as a guide for optimizing device selection in future CMOS technologies. Further research can be carried out by investigating dielectric engineering, strain effects, and work function tuning may also help enhance device reliability under extreme temperature conditions.

REFERENCES

[1] O. Prakash, H. Amrouch, S. Manhas, and J. Henkel, "Impact of NBTI Aging on Self-Heating in Nanowire FET," *Proc. 2020 Des. Autom. Test Eur. Conf. Exhib. DATE 2020*, pp. 1514–1519, 2020, doi: 10.23919/DATE48585.2020.9116267.

[2] S. Tyaginov *et al.*, "Understanding and Modeling Opposite Impacts of Self-Heating on Hot-Carrier Degradation in n- and p-Channel Transistors," *IEEE Int. Reliab. Phys. Symp. Proc.*, vol. 2022-March, pp. 6A31-6A38, 2022, doi: 10.1109/IRPS48227.2022.9764515.

[3] D. Ashique, M. W. Akram, and D. Prasad, "Temperature Variation Comparative Characterization of Nanosheets based FET," *2022 5th Int. Conf. Multimedia, Signal Process. Commun. Technol. IMPACT 2022*, pp. 1–5, 2022, doi: 10.1109/IMPACT55510.2022.10029010.

[4] N. Seoane, K. Kalna, X. Cartoixa, and A. Garcia-Loureiro, "Multilevel 3-D Device Simulation Approach Applied to Deeply Scaled Nanowire Field Effect Transistors," *IEEE Trans. Electron Devices*, vol. 69, no. 9, pp. 5276–5282, 2022, doi: 10.1109/TED.2022.3188945.

[5] Y. Atalla, M. H. Mamat, and Y. Hashim, "Characterization and Optimization of Si0.75Ge0.25-FinFETs Based on Operating Temperature and Gate Length," *J. Nano-Electron. Phys.*, vol. 17, no. 2, pp. 177–185, 2025, doi: 10.21272/jnep.17(2).02011.

[6] G. I. Zebrev and D. S. Malich, "Analytical Physics-Based Modeling of Electron Channel Density in Nanosheet and Nanowire Transistors," *IEEE Trans. Electron Devices*, vol. 70, no. 4, pp. 1574–1579, 2023, doi: 10.1109/TED.2023.3245571.

[7] J. Wu, H. Qi, and Q. Zhao, "Self-Heating Effect of Gate-All-Around FETs: A Review," *Appl. Comput. Eng.*, vol. 168, no. 1, pp. 127–138, 2025, doi: 10.54254/2755-2721/2025.24442.

[8] N. Rangarajan, J. Knechtel, N. Limaye, O. Sinanoglu, and H. Amrouch, "A Novel Attack Mode on Advanced Technology Nodes Exploiting Transistor Self-Heating," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 41, no. 11, pp. 4134–4144, 2022, doi: 10.1109/TCAD.2022.3197496.

[9] V. Kumar, J. Patel, A. Datta, and S. Dasgupta, "Study of Self Heating Effect in the wake of complete and partial bottom dielectric insertion under 5 nm Stacked Nanosheet Transistor," *Memories - Mater. Devices, Circuits Syst.*, vol. 4, no. December 2022, p. 100056, 2023, doi: 10.1016/j.memori.2023.100056.

[10] I. Myeong, Q. Nguyen-Gia, and I. Song, "Self-Heating-Based channel thermal noise of advanced Sub-5-nm-Node nanosheet FET," *Results Phys.*, vol. 67, no. November, p. 108059, 2024, doi: 10.1016/j.rinp.2024.108059.

[11] Y. Atalla, M. H. Mamat, and Y. Hashim, "Characterization of Si0.25Ge0.75-FinFET as a Temperature Nano Sensor," *J. Electron. Electromed. Eng. Med. Informatics*, vol. 7,

no. 2, pp. 422–430, 2025, doi: 10.35882/jeeemi.v7i2.695.

[12] Y. Atalla, M. H. Mamat, and Y. Hashim, "Characterization and Optimization of Si0.75Ge0.25-FinFETs Based on Operating Temperature and Gate Length," *J. Nano-Electron. Phys.*, vol. 17, no. 2, pp. 1–7, 2025, doi: 10.21272/jnep.17(2).02011.

[13] V. M. Van Santen, P. R. Genssler, O. Prakash, S. Thomann, J. Henkel, and H. Amrouch, "Impact of Self-Heating on Performance, Power and Reliability in FinFET Technology," *Proc. Asia South Pacific Des. Autom. Conf. ASP-DAC*, vol. 2020-January, pp. 68–73, 2020, doi: 10.1109/ASP-DAC47756.2020.9045582.

[14] Y. Hashim, "Temperature Characteristics of 10nm N- and P-Channel Si-FinFET Structure," *ICEECIT 2022 - Proc. 2022 Int. Conf. Electr. Eng. Comput. Inf. Technol.*, pp. 104–107, 2022, doi: 10.1109/ICEECIT55908.2022.10030376.

[15] S. P. R. Mallem, P. Puneetha, Y. Choi, S. M. Baek, S. J. An, and K. S. Im, "Temperature-Dependent Carrier Transport in GaN Nanowire Wrap-Gate Transistor," *Nanomaterials*, vol. 13, no. 10, 2023, doi: 10.3390/nano13101629.

[16] H. Jung, "Subthreshold swing model using scale length for sub-10 nm junction-based double-gate MOSFETs," *Int. Journ. of Elect. and Electron. Eng. & Tel.*, vol. 10, no. 2, pp. 1747–1754, 2020, doi: 10.11591/ijece.v10i2.pp1747-1754.

[17] A. Kumar, A. Kumar, and S. Member, "Comprehensive Investigation of Truncated Fin GaN FinFET for Improved Analog / RF Performance," *IEEE Open J. Nanotechnol.*, vol. 6, no. September, pp. 123–130, 2025, doi: 10.1109/OJNANO.2025.3616955.

[18] N. Boukortt, S. Patanè, and G. Crupi, "3D Investigation of 8-nm Tapered n-FinFET Model 3D Investigation of 8-nm Tapered n-FinFET Model," *Silicon*, vol. 12, pp. 1585–1591, July, 2020, doi: 10.1007/s12633-019-00253-y.

[19] M. Mustafa, T. A. Bhat, and M. R. Beigh, "Threshold Voltage Sensitivity to Metal Gate Work-Function Based Performance Evaluation of Double-Gate n-FinFET Structures for LSTP Technology," *World J. Nano Sci. Eng.*, vol. 03, no. 01, pp. 17–22, 2013, doi: 10.4236/wjnse.2013.31003.

[20] A. Mahmood, W. A. Jabbar, Y. Hashim, and H. Bin Manap, "Effects of downscaling channel dimensions on electrical characteristics of InAs-FinFET transistor," *Int. J. Electr. Comput. Eng.*, vol. 9, no. 4, pp. 2902–2909, 2019, doi: 10.11591/ijece.v9i4.pp2902-2909.

[21] C. C. Wu, "Silicon Nanowires Length and Numbers Dependence on Sensitivity of the Field-Effect Transistor Sensor for Hepatitis B Virus Surface Antigen Detection," *Biosensors*, vol. 12, no. 2, 2022, doi: 10.3390/bios12020115.